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| **Course Code:ECE2002** | **Course Title:** Computer Organization and Architecture | | | | **TPC** | **3** | **0** | **3** |
| **Version No.** | **1.0** | | | | | | | |
| **Course Pre-requisites/ Co-requisites/** | **ECE1003** | | | | | | | |
| **anti-requisites (if any).** | **None** | | | | | | | |
| **Objectives:** | 1. Introduction and overview of basic computer organization. Computer arithmetic: binary, hexadecimal and decimal number conversions, binary number arithmetic and IEEE binary floating point number standard. 2. To learm basic computer logic: gates, combinational circuits, sequential circuits, adders, ALU, SRAM and DRAM. 3. To learn basic assembly language programming, basic Instruction Set Architecture (ISA), and the design of single cycle CPU. | | | | | | | |
| **Expected Outcome:** | On completion of the course, students will have the ability to   1. Apply different formats of data representation and number systems, 2. Use Boolean algebra as related to designing computer logic, including solving Karnaugh maps, 3. Design and evaluate combinational and sequential logic circuits with multiple inputs and outputs, 4. Design simple combinational and sequential logic circuits, using a small number of logic gates, 5. Assemble a simple computer with hardware design including data format, instruction format, instruction set, addressing modes, bus structure, input/output, memory, Arithmetic/Logic unit, control unit, and data, instruction and address flow, 6. Design simple assembly language programs that make appropriate use of a registers and memory. | | | | | | | |
| **Module No. 1** | Computer Evolution & Arithmetic | | 8 Hours | | | | | |
| A Brief History of computers, Basic structures of Computers: Computer Architecture vs. Computer Organization, Functional units, Operational concepts, Registers, Bus and Bus organization, Memory location and addresses, Fixed and Floating point numbers, Signed numbers, Integer Arithmetic, 2’s Complement method for multiplication, Booths Algorithm, Hardware Implementation, Division, Restoring and Non Restoring algorithms | | | | | | | | |
| **Module No. 2** | The Central Processing Unit | | 8 Hours | | | | | |
| Basic Processing Units: Fundamental concepts, Instruction format, Instruction set, Addressing  modes. Instruction Sequencing, Execution cycle, Hardwired control, Micro programmed  control. | | | | | | | | |
| **Module No. 3** | Memory Organization | | 6 Hours | | | | | |
| Memory System: Basic Concepts, Memory hierarchy, Main Memory, Secondary storage, Cache  memory. | | | | | | | | |
| **Module No. 4** | ALU | | 8 Hours | | | | | |
| Arithmetic: Addition and Subtraction of signed and unsigned numbers, Multiplication of signed and unsigned numbers, Booth Multiplier, Array Multiplier, Integer Division, Floating- point Numbers and operations. | | | | | | | | |
| **Module No. 5** | I/O Organization | | | 8 Hours | | | | |
| Microprocessors, Instruction set, Assembly Language Programming, Stack, Subroutine,  Interrupt, Accessing I/O devices, Standard I/O Interfaces- RS-232C, IEEE-488, USB, Data  Transfer techniques. | | | | | | | | |
| **Module No. 6** | Parallel Organization | 6 Hours | | | | | | |
| Instruction level pipelining and Superscalar Processors, Multiple Processor Organizations, Closely and Loosely coupled multiprocessors systems, Symmetric Multiprocessors, Clusters, UMA NUMA, Vector Computations,  RISC: Instruction execution characteristics, RISC architecture and pipelining. RISC Vs CISC | | | | | | | | |
| **Text Books**.   1. M. Morris Mano, Rajib Mall, Computer System Architecture, Pearson Education Third Edition,2017 | | | | | | | | |
| **References**   1. Carl Hamacher, Zvonkovranesic, Safwat Zaky, Computer Organization, McGraw Hill,Fifth Edition,2011. 2. William Stallings, Computer Organization and Architecture: Designing for Performance, Pearson Education,Tenth Edition,2013. | | | | | | | | |
| **Mode of Evaluation** | **Practice Tests-20%, Continuous Assessment Tests-60%, Practical Assesment-20%**  Practice Tests - Cumulative for 16 Weeks 20%  Continuous Assessment Test-1 20%  Continuous Assessment Test-2 20%  Continuous Assessment Test-3 20%  Practical Assessment (Mini Project) 20% | | | | | | | |
| **Recommended by the Board of Studies on** | 30-06-2018 | | | | | | | |
| **Date of Approval by the Academic Council** | 2nd Academic Council 21.07.2018 | | | | | | | |